

APPLICATION FOR UNITED STATES LETTERS OF PATENT

FOR

VARIABLE TEMPERATURE AND DOSE ATOMIC LAYER DEPOSITION

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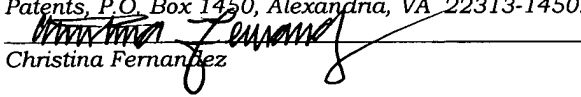
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VARIABLE TEMPERATURE AND DOSE ATOMIC LAYER DEPOSITION

BACKGROUND

1. Field

[0001] Embodiments of the present invention relate to integrated circuits and, in particular, to integrated circuit fabrication processes.

2. Discussion of Related Art

[0002] It is common to use a process known as atomic layer deposition (ALD) to deposit films on semiconductor wafers to fabricate transistors, for example. In ALD, the semiconductor (e.g., silicon, germanium) wafer is placed in a reactor. A precursor material is pulsed into the reactor. The precursor material subsequently adsorbs and reacts on the wafer surface. The precursor material may be any one of hundreds of possible materials, , depending on the reaction product (i.e., metal oxide film, metal nitride film, etc.) desired. The reactor is then purged with an inert gas to remove the precursor material. A second reactant material is pulsed into the reactor. The second reactant material reacts with the precursor material on the wafer surface. Selection of the second reactant material depends on the reaction product desired and on which precursor material was selected. The reactor is purged again.

[0003] This process of precursor pulsing, reactor purging, reactant pulsing, and reactor purging is called a “cycle.” In ALD, the thickness of the deposited film is controlled by the number of cycles.

[0004] In current ALD processes, where metal oxide films are to be deposited on silicon wafers, the films are deposited using preset conditions for the reactor and materials used that remain constant throughout the deposition process. There are drawbacks to using preset conditions, however.

[0005] For example, using one discrete set of preset conditions may produce a film that has good insulation against current leakage but also causes silicon oxide or metal silicate at the interface between the silicon wafer surface and the metal oxide film to be formed. Interfacial silicon oxide or metal silicate can be problematic because these materials have relatively low permittivity, which reduces the effective dielectric constant of a transistor's gate stack.

[0006] A reduced effective dielectric constant results in reduced capacitance, which reduces transistor drive current for a given dielectric film thickness. When the transistor drive current is reduced the speed performance of the device degrades. Using another discrete set of preset conditions may produce a film having very little to essentially no interfacial silicon oxide or metal silicate

but produces a film with poor insulation against current leakage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally equivalent elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the reference number, in which:

[0008] Figure 1 is a high-level block diagram of a system suitable for depositing a film on a substrate according to an embodiment of the present invention;

[0009] Figure 2 is a flowchart illustrating an approach to depositing a film on a substrate according to an embodiment of the present invention;

[0010] Figure 3 is a cross-section view illustrating a metallic film deposited on a substrate according to an embodiment of the present invention;

[0011] Figure 4 is a cross-section view illustrating a transistor fabricated according to embodiments of the present invention; and

[0012] Figure 5 is a high-level block diagram of an optical system according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0013] Figure 1 is high-level block diagram of a variable temperature and dose atomic layer deposition (VTD-ALD) system 100 suitable for implementing embodiments of the present invention. The system 100 includes a reactor 102 for receiving a wafer 104 during deposition of films (e.g., metallic films).

[0014] The VTD-ALD system 100 also includes a reactant 106 coupled to the reactor 102 via a valve 130, a reactant 108 coupled to the reactor 102 via a valve 132, a carrier/purge gas 110 coupled to the reactor 102 via a valve 134, and a carrier/purge gas 112 coupled to the reactor 102 via a valve 136. A controller 120 may be coupled to the valves 130, 132, 134, and 136 to control the flow of reactant 106, the reactant 108, the carrier/purge gas 110, the carrier/purge gas 112, respectively into the reactor 102.

[0015] The reactor 102 may include a heater 114. The controller 120 may be coupled to the heater 114 to control the operation the heater 114 to modulate the temperature of the reactor 102 during the film deposition process.

[0016] The VTD-ALD system 100 may include a vacuum pump 122, which may be coupled to the reactor 102. The controller 120 may be coupled to the vacuum pump 122 to control the operation of the vacuum pump 122.

[0017] The reactor 102 may be any suitable ALD reactor. ALD reactors suitable for implementing the reactor 102 are well known.

[0018] The wafer 104 may be any suitable wafer or substrate. The wafer 104 may be a silicon wafer. Other suitable materials may be used to implement the wafer 104 and after reading the description herein persons of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention for other materials.

[0019] In one embodiment, the reactant 106 may be aluminum-based (e.g., $\text{Al}(\text{CH}_3)_3$), Ti-based, Zr-based, Hf-based, Ta-based, etc. Of course, the reactant 106 depends on the film to be deposited and after reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention using various reactants or precursors.

[0020] In one embodiment, the reactant 108 may be oxygen-based (e.g., H_2O ,

O₂, O₃, H₂O₂, CH₃OH, C₂H₅OH, etc.), nitrogen-based (e.g., NH₃, etc.), or other suitable precursor material. Of course, the reactant 108 depends on the film to be deposited and after reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention using various reactants.

[0021] The carrier/purge gas 110 may be any gas that does not react with the reactant 106. In embodiments of the present invention, the carrier/purge gas 110 may be argon (Ar), nitrogen (N₂), and helium (He). Suitable carrier materials are well known and after reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention using various carrier/purge materials.

[0022] The carrier/purge gas 112 may be any gas that does not react with the reactant 106 or reaction products (e.g., metal films). In one embodiment, the carrier/purge gas 112 is the same as the carrier/purge gas 110. In other embodiments, the carrier/purge gas 112 is different from the carrier/purge gas 110. Suitable carrier/purge materials are well known and after reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention using various carrier/purge materials.

[0023] The heater 114 may be any capable of heating the reactor 102 to a specified temperature. Heaters used in film deposition equipment are well known.

[0024] The controller 120 may be any suitable analog, digital, software, hardware, firmware, etc., (e.g., a microprocessor, a microcontroller) controller that performs VTD-ALD processes according to embodiments of the present invention. For example, the controller 120 may control operation of the valve 130, the valve 132, the valve 134, and the valve 136 to modulate the flow rate of materials into the reactor 102 during the film deposition process.

[0025] The vacuum pump 122 may be any suitable pump capable of removing exhaust gases from the reactor 102. Vacuum pumps used in film deposition equipment are well known.

[0026] Figure 2 is a flowchart illustrating a VTD-ALD process 200 according to an embodiment of the present invention. The process 200 is only an example process and other processes may be used. Additionally, the order in which operations are described should not be construed to imply that the operations are necessarily order-dependent or that the operations be performed in the

order in which they are presented. A machine-accessible medium with machine-accessible instructions thereon may be used to cause the controller 120 or other machine to perform the process 200 or portions thereof.

[0027] In a block 202, a first set of ALD conditions are established. For example, a first set of material (i.e., the reactant 106, the reactant 108, the carrier/purge gas 110, and the carrier/purge gas 112) flow rates are established, a first reactor 102 temperature is established, a first reactor 102 pressure is established, and a first number of cycles to be run is established.

[0028]— In one embodiment, the first reactant 106 flow rate may be established at around approximately 100-300 standard cubic centimeters per minute (SCCM). However, the actual flow rate will depend on the materials to be deposited, the size of the reactor, and other factors. In one embodiment, the first reactant 108 flow rate may be established at around 5-50 SCCM.

[0029] In one embodiment, the first flow rate of the carrier/purge gas 110 may be established at around approximately 500-700 SCCM and the first flow rate of the carrier/purge gas 112 at around approximately 500-700 SCCM.

[0030] Of course, the individual flow rates for the reactant 106, the reactant

108, the carrier/purge gas 110, and/or the carrier/purge gas 112 may range from very small (e.g., around approximately one SCCM) to very large (e.g., in excess of approximately ten thousand SCCM). Optimal flow rates for ALD materials depend on the size of the reactor used, the particular precursor, the particular reactant, the desired deposition rate, and desired film properties. After reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention for various first flow rates.

[0031] In one embodiment, the first temperature of the reactor 102 may be established at 200 degrees Centigrade (200C). Of course, the particular first temperature may be established at anywhere from approximately room temperature to the decomposition temperature of the particular materials used. After reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention for various first temperatures.

[0032] In one embodiment, the first reactor 102 pressure may be established at less than or equal to approximately ten torr. Of course, the particular first pressure depends on the size of the reactor used, the particular precursor, the particular reactant, the desired deposition rate, and desired film properties.

After reading the description herein a person of ordinary skill in the relevant art will readily recognize how to implement embodiments of the present invention for various first temperatures.

[0033] In one embodiment, the first number of cycles to be run is established at twenty. Because the first number of cycles run determines the first depth, greater or fewer cycles may be used depending on the desired depth for the first set of properties.

[0034] In a block 204, the first set of cycles is run using the first set of ALD conditions. In one embodiment, the carrier/purge gas 110 flow is started. For each cycle, the reactor 102 is pulsed with the reactant 106. The reactant 106 reacts with the surface of the wafer 104. The reactor 102 is then purged with the carrier/purge gas 112 to remove any chemically active reactant 106. The reactor 102 is pulsed with the reactant 108, which reacts with the reactant 106 and the wafer 104. The reactor 102 again is purged with the carrier/purge gas 112 to remove any chemically active reactant 108. The first depth is grown in a layer-by-layer manner such that running the first set of cycles yields twenty monolayers of growth.

[0035] In a block 206, the process 200 determines whether to modulate the

film properties. If it is not appropriate to modulate the properties of the film, the reactor 102 is cooled in a block 208 and a film is produced having a depth corresponding to the number of cycles run and the properties corresponding to the first set of ALD conditions. If it is appropriate to modulate the properties of the film, the process 200 proceeds to a block 210.

[0036] It may be appropriate to modulate the properties of the film when the reactant 106 is trimethyl aluminum ($\text{Al}(\text{CH}_3)_3$), the reactant 108 is water (H_2O), the temperature of the reactor 102 is 200C, and twenty cycles are run. This is because the interface between the silicon (Si) wafer and the beginning growth of an alumina (Al_2O_3) film produced by the trimethyl aluminum ($\text{Al}(\text{CH}_3)_3$) and the silicon (Si) may be substantially free from silicon oxide or metal silicate, however, under these same ALD conditions, the first set of monolayers in the film have reduced insulating capabilities as a result of contaminants introduced by unreacted reactant 106/reactant 108 materials. The reduced insulation results in inappropriately high current leakage in devices.

[0037] If it is decided to modulate the properties of the film, in a block 210, a new set of ALD conditions are established. For example, a new set of material (i.e., the reactant 106, the reactant 108, the carrier/purge gas 110, and the carrier/purge gas 112) flow rates may be established, a new reactor 102

temperature may be established, a new reactor 102 pressure may be established, and/or a new number of cycles to be run may be established. In embodiments of the present invention, establishing the first and new sets of conditions may be continuous, incremental, increasing, decreasing, reversing, etc.

[0038] Typically, the carrier/purge gas 110 and the carrier/purge gas 112 flow rates remain constant. Also, the reactor 102 pressure may remain constant. However, changing the reactant 106 flow rate, the reactant 108 flow rate, and/or the reactor 102 temperature each may have a different effect on the properties of the next set of monolayers.

[0039] In one embodiment, the new reactant 106 flow rate is established at closer to around approximately 250 SCCM, the new reactant 108 flow rate is established at closer to around approximately twenty SCCM, the new temperature of the reactor 102 is established at approximately 300C, and the new number of cycles to be run is established to be forty.

[0040] In a block 212, the new number of cycles is run using the new set of ALD conditions. In one embodiment, forty cycles are run using the new set of conditions. For each cycle, the reactor 102 is pulsed with the reactant 106. The

reactant 106 reacts with the surface of the wafer 104. The reactor 102 is then purged with the carrier/purge gas 112 to remove any chemically active reactant 106. The reactor 102 is pulsed with the reactant 108, which reacts with the reactant 106 and the wafer 104. The reactor 102 again is purged with the carrier/purge gas 112 to remove any chemically active reactant 108. The next depth is grown in a layer-by-layer manner such that running the next set of cycles yields forty monolayers of growth.

[0041] It may be appropriate to stop the process 200 at this point when the reactant 106 is trimethyl aluminum ($\text{Al}(\text{CH}_3)_3$), the reactant 108 is water (H_2O), the temperature of the reactor 102 is 300C, and forty cycles are run. Because the interface between the silicon (Si) wafer and the beginning growth of an alumina (Al_2O_3) film is substantially free from silicon oxide or metal silicate, and the new set of monolayers in the film have good insulating capabilities (i.e., at the higher reactor temperature there are fewer unreacted reactant 106/reactant 108 materials). The films produced according to this embodiment of the present invention also may have low flatband voltage shifts.

[0042] Note that metallic films produced according to embodiments of the present invention can be tailored for a particular application. Films having unique properties produced according to embodiments of the present invention

also can be duplicated.

[0043] After the block 212, the process 200 may return to block 206 and be run iteratively to obtain another set of properties at particular depths for the film. Subsequent sets of ALD conditions may be used to modulate the properties of subsequent sets of film monolayers.

[0044] Figure 3 is a cross-section view of a device 300 having a metallic film 302 deposited on a substrate 304 according to an embodiment of the present invention. The metallic film 302 includes a first set of monolayers 306 and a second set of monolayers 308.

[0045] The first set of monolayers 306 has a depth 310. The second set of monolayers 308 has a depth 312. The metallic layer 302 has a depth 314.

[0046] In one embodiment, the ALD conditions used to deposit the first set of monolayers 306 are different from the ALD conditions used to deposit the second set of monolayers 308. As a result, the electrical properties of the first set of monolayers 306 are different from the electrical properties of the second set of monolayers 308. Thus, the metallic layer 302 has different electrical properties throughout its depth 314.

[0047] Although embodiments of the present invention have been described with respect to depositing only two sets of monolayers, embodiments of the present invention are not so limited. For example, it may be appropriate to have a film whose properties gradually change from top to bottom. In this embodiment, an individual reaction condition (temperature, reactant, reactant flow rate, etc.) may be modulated each subsequent cycle (e.g., there may be one hundred different ALD cycles run each with different ALD conditions resulting in a film having one hundred monolayers each having a different set of properties).

[0048] Figure 4 is a cross-section view illustrating a transistor 400 fabricated according to embodiments of the present invention. The example transistor 400 includes a substrate 402 and a gate dielectric layer 404 formed on the substrate 402. The gate dielectric layer 404 may be a metallic film deposited on the substrate 402 according to embodiments of the present invention.

[0049] The illustrated transistor 400 also includes a gate electrode 406 formed on the gate dielectric layer 404, two vertical sidewall dielectric spacers 408 formed on the sides of the gate dielectric layer 404 and the gate electrode 406, and shallow trench isolation (STI) regions 410 formed in the substrate

402.

[0050] The gate dielectric layer 404 may be any suitable material to insulate the gate electrode 406 from the substrate 402. The gate electrode 406 may be polysilicon or other suitable material. The two vertical sidewall spacers 408 may be any suitable dielectric material. The STI regions 410 may be dielectric material and separate the transistor 400 from other transistors formed on the substrate 400.

[0051] Figure 5 is a high-level block diagram of an optical system 500 according to an embodiment of the present invention. The system 500 includes a transponder 502 coupled to an optical amplifier 504 via an optical fiber 506. The optical amplifier 504 is coupled to a multiplexer 508 via an optical fiber 510. The multiplexer 508 is coupled to a transponder 512 via an optical fiber 514. The transponder 502 includes the device 300 and/or the transistor 400.

[0052] Although only one transponder 502, optical amplifier 504, optical fiber set 506, 510, and 514, multiplexer 508, and transponder 512 are shown, it is common to have numerous transponders, optical amplifiers, optical fiber sets, and multiplexers in optical communication systems. Single units are shown for simplicity. The transponder 502 may transmit optical beams to the

receiver 512. Although not shown for purposes of simplicity, the transponder 502 also may receive optical beams from the transponder 510.

[0053] The optical amplifier 506 may be an erbium (Er) doped fiber amplifier (EDFA). Alternatively, the optical amplifier 506 may be an ytterbium (Yb) doped fiber amplifier, a praseodymium (Pr) doped fiber amplifier, a neodymium (Nd) doped fiber amplifier, or other suitable optical amplifier.

[0054] The multiplexer 508 may be a DWDM multiplexer. Alternatively, the multiplexer 508 may be an add-drop multiplexer.

[0055] Embodiments of the present invention may be implemented using hardware, software, or a combination thereof. In implementations using software, the software may be stored on a machine-accessible medium. A machine-accessible medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form accessible by a machine (e.g., a computer, network device, personal digital assistant, manufacturing tool, any device with a set of one or more processors, etc.).

[0056] For example, a machine-accessible medium includes recordable and non-recordable media (e.g., read only memory [ROM], random access memory

[RAM], magnetic disk storage media, optical storage media, flash memory devices, etc.), as well as electrical, optical, acoustic, or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.).

[0057] The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the embodiments of the invention, as those skilled in the relevant art will recognize. These modifications can be made to embodiments of the invention in light of the above detailed description.

[0058] In the above description, numerous specific details, such as particular processes, materials, devices, and so forth, are presented to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the embodiments of the present invention can be practiced without one or more of the specific details, or with other methods, components, etc. In other instances, well-known structures or operations are not shown or described in detail to avoid obscuring the understanding of this description.

[0059] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, process, block, or characteristic described in connection with an embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification does not necessarily mean that the phrases all refer to the same embodiment. The particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0060] The terms used in the following claims should not be construed to limit embodiments of the present invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of embodiments of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.